EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

This application has been amended in the claims as follows:

In **claim 15**, please delete the seventh paragraph which recites:

"implanting third impurity ions of high concentration of a second conductivity type, using first and second gate electrodes and the first through fourth spacers as a mask, to form third impurity diffusion layers in the PMOS and NMOS regions;"

and insert in its place the following two paragraphs:

-- implanting third impurity ions of high concentration of the second conductivity type in the PMOS region, using the first gate electrode and the first and third spacers as a mask, to form a third impurity diffusion layer in the PMOS region;

implanting fourth impurity ions of high concentration of the first conductivity type in the NMOS region, using the second gate electrode and the second and fourth spacers as a mask, to form a fourth impurity diffusion layer in the NMOS region; --.

In line 1 of **claims 2-14 and 16-20**, delete the limitation of "A method" and insert in its place, -- The method --.

Authorization for this examiner's amendment was given in a telephone interview with applicant's representative, Adam C. Volentine, November 18, 2010.

Allowable Subject Matter

2. Claims 1-20 are allowed.

The following is an examiner's statement of reasons for allowance:

With respect to claims 1-14, the prior art of record neither anticipates nor renders obvious all the limitations of the base claim 1, including: implanting fourth impurity ions of a high concentration into a fourth portion of the semiconductor substrate adjacent to the second gate and the second spacers of the second gate, using the second gate and the first and second spacers as a mask, to form a fourth impurity diffusion region of a first conductivity type; and implanting a fifth impurity ions of a high concentration into a fifth portion of the semiconductor substrate adjacent to the third gate and the second spacers of the third gate, using the third gate and the first and second spacers as a mask, to form a fifth impurity diffusion region of a second conductivity type. Claims 2-14 depend from claim 1, and thus are also allowed for the same reasons.

With respect to claims 15-20, the prior art of record neither anticipates nor renders obvious all the limitations of the base claim 15, including: implanting third impurity ions of high concentration of the second conductivity type in the PMOS region, using the first gate electrode and the first and third spacers as a mask, to form a third impurity diffusion layer in the PMOS region; implanting fourth impurity ions of high concentration of the first conductivity type in the NMOS region, using the second gate electrode and the second and fourth spacers as a mask, to form a fourth impurity diffusion layer in the NMOS region; and annealing and diffusing the impurity diffusion layers to define a single lightly-doped drain (LDD) structure in the NMOS region and a

double LDD structure in the PMOS region . Claims 16-20 depend from claim 15, and thus are also allowed for the same reasons.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abul Kalam whose telephone number is 571-272-8346. The examiner can normally be reached on Monday - Friday, 9 AM - 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO

Customer Service Representative or access to the automated information system, call

800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/A. K./
Examiner, Art Unit 2814

/Phat X. Cao/
Primary Examiner, Art Unit 2814